Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-3: (cancelled)

Claim 4 (previously presented): A multi-service segmentation and reassembly (MS-SAR) integrated circuit, comprising:

a first bus interface;

lookup circuitry;

segmentation circuitry;

reassembly circuitry;

a second bus interface; and

a data path extending from the first bus interface to the lookup circuitry, and from the lookup circuitry to the segmentation circuitry, and from the segmentation circuitry to the reassembly circuitry, and from the reassembly circuitry to the second bus interface, wherein both cell-protocol traffic and packet-protocol traffic pass over the data path from the first bus interface, through the lookup circuitry, through the segmentation circuitry, through the reassembly circuitry and out of the integrated circuit from the second bus interface, the lookup circuitry analyzing the cell-protocol traffic and outputting information that causes the cell-protocol traffic to be processed in a first way by the segmentation circuitry and the reassembly circuitry, the lookup circuitry analyzing the packet-protocol traffic and outputting information that causes the packet-protocol traffic to be processed in a second way by the segmentation circuitry and the reassembly circuitry, wherein the integrated circuit is operable in an ingress mode such that traffic is output from the integrated circuit to a switch fabric via the second bus interface, and wherein the integrated circuit is operable in an egress mode such that traffic is received onto the integrated circuit from a switch fabric via the first bus interface.

Claims 5 to 9: (cancelled)

Claim 10 (previously presented): An integrated circuit comprising:

a first bus interface;

means for generating a segmentation trailer;

means for checking a segmentation trailer;

a second bus interface; and

a data path extending from the first bus interface to the means for generating, and from the means for generating to the means for checking, and from the means for checking to the second bus interface, wherein both cell-protocol traffic and packet-protocol traffic pass over the data path from the first bus interface, through the means for generating, through the means for checking, and out of the integrated circuit from the second bus interface, wherein the integrated circuit is operable in an ingress mode and in an egress mode,

wherein in the ingress mode the integrated circuit is adapted for segmenting a packet into a plurality of segments, the means for generating a segmentation trailer generating a segmentation trailer and appending the segmentation trailer to one of the segments, the segments being output from the integrated circuit in the form of switch cells, and

wherein in the egress mode the integrated circuit is adapted for outputting packet information such that the packet information is transmitted as a packet onto a network, the means for checking receiving a plurality of segments, a last one of the plurality of segments including a segmentation trailer, the means for checking checking the segmentation trailer.

Claim 11 (original): A switching device, comprising:

a first multi-service segmentation and reassembly (MS-SAR) integrated circuit;

a switch fabric; and

a second multi-service segmentation and reassembly (MS-SAR) integrated circuit, a flow of network information passing into the first MS-SAR, and then through the first MS-SAR, and then through the switch fabric, and then through the second MS-SAR, and then out of the second MS-SAR, wherein the flow passing into the first MS-SAR is of a first traffic type, and wherein the flow passing out of the second MS-SAR is of a second traffic type, wherein the switching

device can process the flow for all the four following pairs of first and second traffic types: 1) the first traffic type is ATM and the second traffic type is ATM, 2) the first traffic type is ATM and the second traffic type is packet, 3) the first traffic type is packet and the second traffic type is ATM, and 4) the first traffic type is packet and the second traffic type is packet, wherein the first and second MS-SAR integrated circuits are substantially identical integrated circuits.

Claim 12 (original): The switching device of Claim 1, wherein when the first traffic type is ATM and the second traffic type is packet then the ATM traffic type involves AAL5 adaptation layer cells, and wherein when the first traffic type is packet and the second traffic type is ATM then the ATM traffic type involves AAL5 adaptation layer cells.

Claim 13 (original): The switching device of Claim 11, wherein the switching device can also process a flow such that a single ATM cell is received onto the first MS-SAR and that ATM cell is output from the second MS-SAR encapsulated in a packet, there only being one ATM cell encapsulated in the packet.

Claim 14 (original): The switching device of Claim 11, wherein the switching device can also process a flow such that a packet that encapsulates a single ATM cell is received onto the first MS-SAR, and wherein the ATM cell is de-encapsulated and output from the second MS-SAR as an ATM cell.

Claim 15 (original): The switching device of Claim 11, wherein the switching device is an OSI layer three Internet Protocol (IP) router.

Claim 16 (original): The switching device of Claim 11, wherein the switching device is an OSI layer two switch that does not perform Internet Protocol (IP) routing.

Claims 17 to 44 (cancelled)

Claim 45 (previously presented): The integrated circuit of Claim 4, wherein the integrated circuit

is configurable such that the integrated circuit in the ingress mode can output the traffic to either a cell-based switch fabric or to a packet-based switch fabric, and wherein the integrated circuit is configurable such that the integrated circuit in the egress mode can receive the traffic from either a cell-based switch fabric or a packet-based switch fabric.

Claim 46 (cancelled)

Claim 47 (currently amended): ~~The integrated circuit of Claim 46,~~ An integrated circuit, comprising:

a first bus interface;

a second bus interface; and

means for receiving both cell-protocol traffic and packet-protocol traffic from the first bus interface, for buffering both the cell-protocol traffic and the packet-protocol traffic in a payload memory, and for outputting both cell-protocol traffic and packet-protocol traffic from the payload memory via the second bus interface, the means being operable in either an ingress mode wherein both the cell-protocol traffic and the packet-protocol traffic are output from the integrated circuit to a switch fabric via the second bus interface, or an egress mode wherein both the cell-protocol traffic and the packet-protocol traffic are received onto the integrated circuit from a switch fabric via the first bus interface, wherein in the ingress mode the cell-protocol traffic and the packet-protocol traffic are output from the second bus interface in the form of switch cells, and wherein in the egress mode the cell-protocol traffic and the packet-protocol traffic are received from the switch fabric in the form of switch cells.

Claim 48 (currently amended): ~~The integrated circuit of Claim 46,~~ An integrated circuit, comprising:

a first bus interface;

a second bus interface; and

means for receiving both cell-protocol traffic and packet-protocol traffic from the first bus interface, for buffering both the cell-protocol traffic and the packet-protocol traffic in a payload memory, and for outputting both cell-protocol traffic and packet-protocol traffic from the

payload memory via the second bus interface, the means being operable in either an ingress mode wherein both the cell-protocol traffic and the packet-protocol traffic are output from the integrated circuit to a switch fabric via the second bus interface, or an egress mode wherein both the cell-protocol traffic and the packet-protocol traffic are received onto the integrated circuit from a switch fabric via the first bus interface wherein the integrated circuit is configurable such that the switch fabric to which the cell-protocol traffic and the packet-protocol traffic are output in the ingress mode can be either a cell-based switch fabric or a packet-based switch fabric, and wherein the integrated circuit is configurable such that the switch fabric from which the cell-protocol traffic and the packet-protocol traffic are received in the egress mode can be either a cell-based switch fabric or a packet-based switch fabric.

Claim 49 (currently amended): The integrated circuit of Claim ~~46~~ 47, wherein the means includes a segmentation engine, the segmentation engine being controlled to process the cell-protocol traffic in a first way and to process the packet-protocol traffic in a second way.

Claim 50 (currently amended): The integrated circuit of Claim ~~46~~ 47, wherein the means includes a reassembly engine, the reassembly engine being controlled to process the cell-protocol traffic in a first way and to process the packet-protocol traffic in a second way.

Claims 51-53 (cancelled).

Claim 54 (new): The integrated circuit of Claim 48, wherein the means includes a segmentation engine, the segmentation engine being controlled to process the cell-protocol traffic in a first way and to process the packet-protocol traffic in a second way.

Claim 55 (new): The integrated circuit of Claim 48, wherein the means includes a reassembly engine, the reassembly engine being controlled to process the cell-protocol traffic in a first way and to process the packet-protocol traffic in a second way.